Notice of Allowability	Application No.	Applicant(s)	
	10/711,879	CHOU ET AL.	
	Examiner	Art Unit	
	Nitin Patel	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8/22/2007*.
2. ☒ The allowed claim(s) is/are *1,2,4-9,11-20 Now renumbered 1-18 respectively*.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 7/15/2007
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Nitin Patel

NITIN I. PATEL
PRIMARY EXAMINER

REASON FOR ALLOWANCE

1. Claims 1-2,4-9,11-20 are allowed. Claims 3,10 have been cancelled.

2. Claims 15-19 were allowed in previous office action mailed on 5/22/2007.

The following is an examiner's statement of reason for allowance:

The prior art fails to teach or suggest a thin film transistor array plate, comprising: a substrate, having a display region and a peripheral circuit region; a plurality of pixel structures, disposed inside the display region; a plurality of switching devices, disposed inside the peripheral circuit region; a plurality of lead lines, disposed on the substrate, wherein each one of the lead lines electrically connects to the corresponding pixel structures and one of the switching devices; and **a plurality of electrostatic discharge (ESD) protection circuits, disposed inside the peripheral circuit region, wherein each one of the ESD protection circuits is electrically connected to the corresponding switching devices, wherein the ESD protection circuits comprises: a first electrostatic discharge protection circuit, electrically connected to odd numbered gate lines; a second electrostatic discharge protection circuit, electrically connected to even numbered gate lines; a third electrostatic discharge protection circuit electrically connected to odd numbered source lines; and a fourth electrostatic discharge protection circuit, electrically connected to even numbered source lines** as claimed in claim 1.

The prior art fails to teach or suggest a liquid crystal display panel, comprising: a color filter plate; a thin film transistor array plate, having a display region and a peripheral circuit region, comprising: a plurality of pixel structures, disposed inside the

display region; a plurality of switching devices, disposed inside the peripheral circuit region; a plurality of lead lines, disposed on the substrate, wherein each lead line electrically connects the corresponding pixel structures and one of the switching devices; and a plurality of electrostatic discharge (ESD) protection circuits, disposed inside the peripheral circuit region, wherein each one of the ESD protection circuits is electrically connected to portions of the switching devices; and a liquid crystal layer, disposed between the color filter plate and the thin film transistor array plate. wherein the ESD protection circuits comprises: a first electrostatic discharge protection circuit, electrically connected to odd numbered gate lines; a second electrostatic discharge protection circuit, electrically connected to even numbered gate lines; a third electrostatic discharge protection circuit, electrically connected to odd numbered source lines; and a fourth electrostatic discharge protection circuit, electrically connected to even numbered source lines as claimed in claim 8.

The prior art fails to teach or suggest a thin film transistor array plate, comprising: a substrate, having a display region and a peripheral circuit region; a plurality of gate lines, disposed on the substrate; a plurality of source lines, disposed on the substrate, wherein the gate lines and the source lines define the display region into a plurality of pixel areas; a plurality of thin film transistor, each thin film transistor disposed inside one of the pixel area, wherein each one of the thin film transistors is electrically connected to one of the gate lines and one of the source lines correspondingly; a plurality of pixel electrode, each pixel electrode positioned inside one of the pixel areas and electrically connected to a corresponding thin film transistor; a plurality of switching devices,

disposed inside the peripheral circuit region, wherein each one of the switching devices is electrically connected to one of the gate lines and the source lines; a first electrostatic discharge protection circuit, disposed inside the peripheral circuit region, wherein the first electrostatic discharge protection circuit is electrically connected to odd numbered gate lines through portions of the switching devices; a second electrostatic discharge protection circuit, disposed inside the peripheral circuit region, wherein the second electrostatic discharge protection circuit is electrically connected to even numbered gate lines through portions of the switching devices; a third electrostatic discharge protection circuit, disposed inside the peripheral circuit region, wherein the third electrostatic discharge protection circuit is electrically connected to odd numbered source lines through portions of the switching devices; and a fourth electrostatic discharge protection circuit, disposed inside the peripheral circuit region, wherein the fourth electrostatic discharge protection circuit is electrically connected to even numbered source lines through portions of the switching devices as claimed in claim 15.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 571-272-7677. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin H. Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nitin Patel
Primary Examiner
Art Unit 2629

Nitin Patel

NITIN I. PATEL
PRIMARY EXAMINER